CLAIMS

What is claimed is:

1. A method for forming a copper dual damascene with improved copper migration resistance and improved electrical resistivity comprising the steps of:

providing a semiconductor wafer comprising upper and lower dielectric insulating layers separated by a middle etch stop layer;

forming a dual damascene opening extending through a thickness of the upper and lower dielectric insulating layers wherein an upper trench line portion extends through the upper dielectric insulating layer thickness and partially through the middle etch stop layer;

blanket depositing a barrier layer comprising at least one of a refractory metal and refractory metal nitride to line the dual damascene opening;

carrying out a remote plasma etch treatment of the dual damascene opening to remove a bottom portion of the barrier layer to reveal an underlying conductive area; and,

filling the dual damascene opening with copper to provide a substantially planar surface.

2. The method of claim 1, wherein the middle etch stop layer comprises at least two different material layers including a lowermost layer and an uppermost layer.

3. The method of claim 1, wherein the middle etch stop layer comprises at least two different material layers selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

4. The method of claim 1, wherein the middle etch stop layer comprises a lowermost layer selected from the group consisting of silicon nitride and silicon oxynitride and an uppermost layer selected from the group consisting of silicon carbide, and silicon oxycarbide.

5. The method of claim 1, wherein the middle etch stop layer comprises a silicon oxynitride lowermost layer and a silicon carbide uppermost layer.

6. The method of claim 1, wherein the barrier layer is selected from the group consisting of Ta, Ti, W, TaN, TiN, WN, and TaSiN.

7. The method of claim 1, wherein the barrier layer consists essentially of a Ta/TaN composite layer.

8. The method of claim 1, wherein the PVD process comprises an ion metal plasma (IMP) process.

9. The method of claim 1, wherein the remote plasma etch treatment comprises a remote plasma generator disposed upstream of an etch process chamber.

10. The method of claim 1, wherein the remote plasma etch treatment comprises one of an RF and microwave power source.

11. The method of claim 1, wherein the underling conductive area comprises copper.

12. The method of claim 1, wherein the step of filling the dual damascene opening with copper comprises the steps of:

depositing a copper seed layer;

carrying out an electro-chemical deposition process to fill the dual damascene opening with a copper filling; and,

carrying out a CMP process to remove at least the copper filling portion overlying the dual damascene opening level.

13. A method for forming a copper dual damascene with improved copper migration resistance and improved electrical resistivity comprising the steps of:

providing a semiconductor wafer comprising upper and lower dielectric insulating layers separated by a composite middle etch stop layer;

forming a dual damascene opening extending through a thickness of the upper and lower dielectric insulating layers wherein an upper trench line portion extends through the upper dielectric insulating layer thickness and partially through a thickness of the middle etch stop layer;

blanket depositing a barrier layer comprising at least one of a refractory metal and refractory metal nitride to line the dual damascene opening;

carrying out a remote plasma etch treatment of the dual damascene opening to remove a bottom portion of the barrier layer to reveal an underlying conductive portion; and,

filling the dual damascene opening with copper to provide a substantially planar surface.

14. The method of claim 13, wherein the composite etch stop layer comprises a lowermost layer selected from the group consisting of silicon nitride and silicon oxynitride and an uppermost layer selected from the group consisting of silicon carbide, and silicon oxycarbide.

15. The method of claim 13, wherein the composite etch stop layer comprises a silicon oxynitride lowermost layer and a silicon carbide uppermost layer.

16. The method of claim 13, wherein the barrier layer is selected from the group consisting of Ta, Ti, W, TaN, TiN, WN, and TaSiN.

17. The method of claim 13, wherein the barrier layer consists essentially of a Ta/TaN composite layer.

18. The method of claim 13, wherein the PVD process comprises an ion metal plasma (IMP) process.

19. The method of claim 13, wherein the remote plasma etch treatment comprises a remote plasma generator disposed upstream of an etch process chamber.

20. The method of claim 13, wherein the remote plasma etch treatment comprises one of an RF and microwave power source.

21. The method of claim 13, wherein the underling conductive area comprises copper.

22. The method of claim 13, wherein the step of filling the dual damascene opening with copper comprises the steps of:

depositing a copper seed layer;

carrying out an electro-chemical deposition process to fill the dual damascene opening with a copper filling; and,

carrying out a CMP process to remove at least the copper filling portion overlying the dual damascene opening level.